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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,381	04/08/2004	John P. Plasterer	DATUMTE.018A	7636

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/820,381	PLASTERER ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *5-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 42-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/5/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 42-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldman et al. (6,788,103) in view of Canagasaby et al. (2004/0088594).

Claim 1, Feldman shows an input (dp, Fig. 7) and a differential output (qn, qp), the circuit comprising:

A circuit fabricated in an integrated circuit with a differential a differential circuit with a first NMOS transistor (430) and a second NMOS transistor (404), where the first NMOS transistor has a source, a gate, and a drain, and the second NMOS transistor has a source, a gate, and a drain, where the source of the first NMOS transistor and the source of the second NMOS transistor are coupled (coupled to 401), where the gate of the first NMOS transistor and the gate of the second NMOS transistor are configured to receive the differential input (dp and dn), and where the drain of the first NMOS transistor and the drain of the second NMOS transistor are configured to provide the differential output (qn and qp);

a first current source (401) with at least a first terminal, where the first terminal of the first current source is coupled to the source of the first NMOS transistor and to the source of the second NMOS transistor;

a first active load (407 and 410) with at least a first terminal coupled to the drain of the first NMOS transistor of the differential circuit, where the first terminal of the first active load has an inductive impedance characteristic (active inductor, col. 3, lines 35-47) as seen from the drain of the first NMOS transistor; and

a second active load (411 and 408) coupled to the drain of the second NMOS transistor of the differential circuit, where the second active load has an inductive impedance characteristic (active inductor, col. 3, lines 35-47) as seen from the drain of the second NMOS transistor.

Therefore, Feldman discloses the claimed invention except for the differential circuit, the first current source, the first active load, and the second active load form at least part of a state machine.

Canagasaby shows a state machine (330 and 340 in Fig. 3 are considered as a state machine, [0040] in a micro-processor shows as chip A or B in figures 1A-1B) comprises a differential circuit (Figure 15) having a current source (1540A-D), the first active load (1510, active load [0070]), and the second active load (1512).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the differential circuit of Feldman having the first current source, the first active load, and the second active load as part of a state machine in a micro-processor, in order to extract the phase/frequency information about the remote data clock from the data stream received from the micro-processor communication.

Claim 2, Feldman shows the circuit as defined in Claim 1, where the first current source is an NMOS transistor (transistor 401 is NMOS) with a source, a gate, and a

drain, and where the first terminal of the first current source corresponds to the drain of the NMOS transistor.

Claim 3, Feldman shows the circuit as defined in Claim 1, wherein the first active load and the second active load exhibit the inductive impedance characteristic without benefit of a passive inductor (active inductance, col. 3, lines 35-46).

Claim 4, Feldman shows the circuit as defined in Claim 1, wherein the first active load further comprises:

a third NMOS transistor (407) with a source, a gate, and a drain, where the source corresponds to the first terminal of the first active load, where the drain is coupled to a first voltage reference (Vdd); and a resistance device (410) with a first terminal and a second terminal, where the first terminal of the resistance device is coupled to the gate of the third NMOS transistor, and where the second terminal of the resistance device is coupled to a second voltage reference (Bias1).

Claim 42, Feldman shows an integrated circuit with metal-oxide-semiconductor field- effect transistors (MOSFETS) fabricated on a silicon substrate, the integrated circuit comprising:

a differential logic circuit (Fig. 7) implemented with current-controlled complementary metal-oxide semiconductor field-effect transistor circuits (MOS, col. 4, line 54); and

active loads (407, 410, 411, 408) coupled to the transistor circuits of the differential logic circuit, where the active loads mimic the response of inductors without inclusion of an explicit inductor (active inductor without inductor, col. 3, lines 35-46).

Therefore, Feldman discloses the claimed invention except for the differential circuit and the active load form at least part of a state machine.

Canagasaby shows a state machine (330 and 340 in Fig. 3 are considered as a state machine, [0040] in a micro-processor shows as chip A or B in figures 1A-1B) comprises a differential circuit (Figure 15) with the first active load (1510, active load [0070]), and the second active load (1512).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the differential circuit of Feldman having the first active load, and the second active load as part of a state machine in a micro-processor, in order to extract the phase/frequency information about the remote data clock from the data stream received from the micro-processor communication.

Claim 43, Feldman shows the integrated circuit as defined in Claim 42, wherein the differential logic circuit is configured to correspond to at least a portion of a buffer, an inverter, an AND gate, a NAND gate, an OR gate, a NOR gate, a multiplexer, a latch, or a flip-flop (col. 4, lines 23-38).

Claim 44, Feldman in view of Canagasaby shows the integrated circuit as defined in Claim 42, wherein the state machine is embodied in a microprocessor (microprocessor, chip A or B, Fig. 1A – 1B and [0034]).

Claim 45, Feldman in view of Canagasaby shows the integrated circuit as defined in Claim 42, wherein the state machine is embodied in a graphics processor (graphics [0034]).

Claim 46, Feldman in view of Canagasaby shows the state machine is embodied in a serial-deserializer (inherent limitation in a microprocessor which communicated serially between IC chip 110 and IC chip 120, [0038]).

Claim 47, Feldman in view of Canagasaby shows the integrated circuit as defined in Claim 42, wherein the state machine comprises at least a combination of logic cells (NOR gate and compare, Fig. 10) and a flip-flop (336A, Fig. 10 and page 10, [0121] on the right column and start at line 9).

Claim 48, Feldman in view of Canagasaby shows the circuit as defined in Claim 1, wherein the state machine comprises at least a combination of logic cells and (NOR gate and compare, Fig. 10) and a flip-flop (336A, Fig. 10 and page 10, [0121] on the right column and start at line 9).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Claims 5-41 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/16/05.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

3/14/06